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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,302	07/11/2003	Stefan Honken	59421 (45107)	4333

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EXAMINER
ZAIDI, SYED

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/618,302	HONKEN ET AL.	
	Examiner	Art Unit	
	Syed Zaidi	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed September 25th, 2007 have been fully considered but they are not persuasive.

Consider claims 1, 11, and 12, Applicant argues, on page 6 of the remarks that **Ueda.** do not teach "the adjusting signal depends not only on the phase difference between the clock of the frame transmission and the data clock, but also on a second phase difference for N successive frames". The Examiner respectfully disagrees with Applicant's argument because as recited in the above rejection, **Ueda.** suggests a when the phase of the frame data signal and the clock signal received from the active radio transmitter are different (column 9 Lines 44-45 and figure # 6A-E) from those of the frame data signal and the clock signal directly received from the transmitting data processing unit, the delay time adjuster provided in the transmitting data processing unit adjusts the delay time so that both the phase of the two frame data signals and the two clock signals are coincident with each other (column 36 Lines 1-24 and figure # 1).

The applicants argue on page 7, that **Ueda.** do not teach or suggest the injection or insertion of stuffing bits or stuffing data symbols as recited in independent claims 1, 11, and 12. In particular. The Examiner respectfully disagrees with Applicant's argument because as recited in the above rejection. **Ueda.** suggests One frame referred to as a multiframe is composed of 30 subframes (time slots), and each subframe is composed of 1 bit of control data (overhead bit) Si (i=1 to 30) and 7 bits of information data, as shown in FIG. 36A. A stuffing bit (dummy data) V or input data is inserted into the 30-th subframe (column 1 Lines 43-48 and figure # 36A).

The applicants argue on page 7, that **Ueda.** does not teach or suggest that the adjusting signal is produced depending on the phase difference determined from N successively transmitted frames. The Examiner respectfully disagrees with Applicant's argument because as recited in the above rejection. **Ueda.** Suggests A received data processing unit 45 executes phase difference comparison, deframing and other processing, and a U-B converter 46 converts a unipolar signal into a bipolar signal and inputs it to a demultiplexer DMPX (column 14 Lines 46-67 and figure # 3).

The applicants argue on page 8 that neither **Ueda.** nor **Hirosaki et al.,** do not teach all the elements of claim 15 and 17 depend from claim 12. The Examiner respectfully disagrees with Applicant's argument because as recited in the above rejection. **Ueda.** is a primary reference and **Hirosaki et.,** teaches a second synchronizing signal regenerator 197 is similar to the synchronizing signal regenerator 192 and is supplied with the SS signal from the up transmission line 43(1) through a branch 197'. Responsive to PN clocks and frame synchronizing signals (column 13 Lines 41-60 and figure # 9 and elements 133, 96) regenerated by the second synchronizing signal regenerator 197 and controlled by the address signal supplied from the address input terminal 62, first through q-th modulation M sequence generators 198(1) to 198(q) generate first through q-th frame synchronized component M sequences of the second q-th-family M sequence (column 29 Lines 65-67 and column 30 Lines 1-10 and figure # 9). First through q-th modulation multipliers 199(1) to 199(q) connected in series correspond to the second multiplier 72 (column 47 Lines 20-42).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-14 and 16 are rejected under 35 U.S.C. 102(b) as being unpatentable by **Ueda. (**US.Patent Number: 5,708,684).

Consider Claims 1, and **12**, **Ueda.** method for controlling the phase of successively transmitted frames (Column 8 lines 11-25, Column 8 lines 44-48), in which data symbols are transmitted at a constant symbol frequency (Column 6 lines 40-44) in which method a phase difference (Column 8 lines 9-15 and figures 46) between the clock (Column 6 lines 29-35) of the frame transmission and a data clock is determined (Column 6 lines 33-44) and dependent on the phase difference an adjusting signal is produced for controlling the injection of stuffing data symbols (Column 8 lines 44-48) into the frames for changing the frame length and the phase of the frame

transmission whereby the phase of the frame transmission is controlled so that the frames are transmitted on average synchronously (Column 4 lines 33-37, and figure # 38 element 0) with the data clock (Column 8 lines 22-24, Column 8 lines 29-34) wherein the adjusting signal is produced dependent on the phase difference (Column 12 lines 20-38 and figure # 2A & 2B) and determined from N frames in each case successively transmitted whereby N is at least equal to 2 (Column1 lines 57-60 and figure # 36 B).

Consider Claims 2 and **13,** as applied to claim 1 and 12 above**, Ueda.** clearly shows and discloses a method for controlling (wherein the controlling, according to which the adjusting signal is produced, has a proportional section and an integral section) according to which the adjusting signal is produced, has a proportional section and an integral section (Column 2 lines 56-62, Column 8 lines 25-48).

Consider Claims 3 and **14,** as applied to claim 1 and 12 above, **Ueda.** clearly shows and discloses a method for controlling of the adjusting signal has a large limit cycle (Column 2 lines 56-62).

Consider Claim 4, and as applied to claim **1** above, **Ueda.** clearly show a method, wherein the controlling of the adjusting signal (Column 7 lines 1-10) is set up in such a manner that it has a large limit cycle and a small limit cycle (Column 2 lines 56-62) the adjusting signal movement of which has a higher frequency than the adjusting signal movement of the large limit cycle and during which stuffing (Column 1 lines 53-60) data symbols are injected in two alternating amounts (Column 2 lines 1-7) into the frames.

Consider Claim 5, and as applied to claim **1** above, **Ueda.** clearly shows and discloses method, wherein the adjusting signal can assume several different conditions, whereby the different conditions designate different amounts of injected stuffing data symbols (Column 1 lines 43-48).

Consider Claim 6, and as applied to claim **1** above, **Ueda.** clearly shows and discloses a method, wherein the adjusting signal is produced dependent on the phase difference averaged in each case over N frames successively transmitted (Column 1 lines 57 – 67, Column 2 lines 1-7).

Consider Claim 7, and as applied to claim **1** above, **Ueda.** clearly shows and discloses a method for controlling of the adjusting signal is time and amplitude discrete (Column 8 lines 48-62).

Consider Claim 8, and as applied to claim **1** above, **Ueda.** clearly shows a method, wherein for determining the phase of the transmitted frames and the data clock or for determining the phase difference (Column 8 lines 34-48), thereof it is recorded in which periods of a signal with a phase measurement frequency an edge of the data clock or the beginning of a new frame arises (Column 8 lines 34-38).

Consider Claim 9, and as applied to claim **8** above, **Ueda** clearly show and disclose a method for determining the phase measurement frequency is an integral multiple of the symbol frequency (Column 6 lines 40-44, Column 16 lines 37-43).

Consider Claim 10, and as applied in claim **1** above, **Ueda.** disclose the claimed invention to show and disclose a method wherein, N is equal to 2 (Column 1 lines 57-61, Column 2 lines 1-7).

Consider Claim 11, **Ueda.** clearly show and disclose a device, phase detector for use in a device for controlling the phase of successively transmitted frames (Column 8 lines 34-48) in which data symbols are transmitted at a constant symbol frequency (Column 6 lines 41-44) whereby the phase detector is set up in such a manner that it determines a phase difference between the clock of the frame transmission and a data clock and produces an output signal (Column 8 lines 22-48) where by the phase detector is set up in such a way that it produces the output signal dependent on the phase difference determined from N frames in each case

successively transmitted, whereby N is at least equal to 2 and whereby the controlling device is set up in such a manner that dependent on the output signal of the phase detector an adjusting signal is produced for controlling the injection of stuffing data symbols into the frames for changing the frame length and the phase of the frame transmission and controls the phase of the frame transmission so that the frames on average are transmitted synchronously with the data clock (Column 1 lines 57-61, Column 2 lines 1-7).

Consider Claim 16, and as applied in claim 12 above, **Ueda.** disclose the claimed invention and clearly show and disclose a device, wherein the signals are processed digitally in the device (Column 8 lines 22-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the

time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable by **Ueda.** (U.S. Patent Number: 5,708,684) in view of **Hirosaki et al.** (U.S. Patent Number: 4,392,220).

Consider Claim 15, and as applied in claim 12 above, **Ueda.** disclose the claimed invention except the device is integrated in a semiconductor module.

In the same field of endeavor, **Hirosaki et al.** disclose a method wherein device is integrated in a semiconductor module (Column 54 lines 60-61 and figure # 35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to incorporate program in a microprocessor as taught by **Hirosaki et al.** with the method of **Ueda.** in order to synchronize the amplitude because the differential amplifiers are readily implemented as an integrated semiconductor circuit.

Consider Claim 17, as applied in claim 12 above, **Ueda.** disclose the claimed invention except the signals are processed in the device by execution of a program in a microprocessor.

In the same field of endeavor, **Hirosaki et al.** disclose a method wherein the signals are processed in the device by execution of a program in a microprocessor (Column 33 lines 1-9).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to incorporate program in a microprocessor as taught by **Hirosaki et al.** with the method of **Ueda.** in order to synchronize upstream clock to the master clock signal.

Conclusion

THIS ACTION IS MADE FINAL

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the

event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Syed Zaidi whose telephone number is (571) 270-1779. The Examiner can normally be reached on Monday-Thursday from 6:30am to 5:00pm. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100. Any inquiry of a general nature or relating to the status of this application or proceeding should be

directed to the receptionist/customer service whose telephone

number is (571) 272-2600.

Syed S. Zaidi

Syed Zaidi
S.Z/s.z
November 30th, 2007.

Seema S. Rao 12/10/07
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